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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,603	10/17/2001	Robert F. Dvorak	NBD-48/47181-00259	7891

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SQUARE D COMPANY
INTELLECTUAL PROPERTY DEPARTMENT
1415 SOUTH ROSELLE ROAD
PALATINE, IL 60067

EXAMINER
BENENSON, BORIS

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/981,603	Applicant(s) DVORAK ET AL.	
	Examiner Boris Benenson	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 12,27,39 and 41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear how test signal buffer 106 will drive a test winding 45, if group of two inversely connected diodes is shunting winding 45 of di/dt sensor and what kind of the signal should be provided from buffer 106.

Claim Rejections - 35 USC § 102

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1-3,5-7,10-11,16-18,20-23, 25-26, 28-30 and 32-35,37-38 are rejected under 35 U.S.C. 102(a) as being anticipated by Haun et al. (6,259,996).

Referring to Claims 1,16 and 28, Haun et al. disclose an ARC Fault Detection System, which produce a trip signal for

circuit breaker or other interrupting device, detecting arcing faults in an electrical circuit. System include a circuit for "*sensing a change in current in said circuit and developing a corresponding input signal, analyzing said input signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal and processing said current signal and said output signal in a predetermined fashion to determine whether an arcing fault is present in said circuit*"(Col.2, Lines 8-14). System includes also a microcontroller running an algorithm for analyzing the output signal for current peaks and current rise time. "*To distinguish between normally noisy load currents and arcing currents, the algorithm looks for different levels of (di/dt) broadband noise, high currents, decaying currents and current aspect ratios*" (Col.5, Lines 39-43). Haun et al. disclose, "*all of the components of the arcing fault circuit detector, the current fault detector circuit and the ground fault detector circuit, as well as some other circuit components to be described later, are provided on an application specific integrated circuit (ASIC)" (Col.3, Lines 39-43).*

Referring to Claims 2,17 and 29, Haun et al. disclose a "*controller including a plurality of counters and wherein said controller increments said plurality of counters in a*

predetermined fashion in accordance with said input signals and periodically determines whether an arcing fault is present based at least in part on the state of said plurality of counters" (Col.2, Lines 33-37).

Referring to Claims 3,18 and 30, Haun et al. disclose, "*the controller increments a plurality of counters, which may be implemented in software, in accordance with the input signals received from the ASIC*" (Col.5, Lines 30-32).

Referring to Claim 5,20 and 32, Haun et al. disclose presence of a microcontroller, which implements a software and firmware counters. It is inherence that such microcontroller comprises a microprocessor.

Referring to Claims 6-7,21-23 and 33-35, Haun et al. disclose a broadband noise detector. "*The broadband noise detector 24 (Fig.1) comprises first and second band-pass filter circuits 80, 82 which receive the rate of change of current signal from the di/dt sensor 16" (Col.3, Lines 54-56). "The threshold detectors 84 and 86 are responsive to those components of the frequency signals passed by the band-pass filters 80 and 82 which are above a predetermined threshold amplitude for producing a corresponding frequency amplitude output to signal conditioning circuits 88 and 90. These circuits 88 and 90 produce a conditioned output signal in a form suitable for input*

into the microcontroller 40" (Col.4, Lines 3-10). A simultaneous output of circuits 88 and 90 through AND circuit 96 directed to increment a counter in the microcontroller.

Referring to Claims 10-11,25-26 and 37-38, the microcontroller (40) is generating "trip_signal", which in turn open up the line contact (47) of the circuit interrupter (44). It is inherent that the interrupter latches and requires to be reset for further operations. The use of a buffer (capacitor) in order to accumulate energy and utilize stored energy is routine and should be claimed as an invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4,19 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view Miller (4,792,899). Haun et al. disclose an ARC Fault Detection System. All claim limitations of Claim 1 have been discussed above. Claim 4 adds onboard DC voltage regulator for supplying voltage

for all of the analog and digital circuits on the integrated chip. Haun et al. is silent about that subject. Miller teaches microprocessor support integrated circuit that includes a voltage regulator, providing regulated voltage for all digital and analog circuitry on the chip. It would have been obvious to one of ordinary skill in the art at the time the invention to include voltage regulator on the chip because it will provide integrity of output and prevent false occurrence of false signals, especially during power up time or due a "noise" in the power line.

3. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view of Lee at al. (5,774,555). As we discussed earlier in reference to Claims 6-7, Haun et al. disclose a broadband noise detector including at least two bandpass filters for different passbands, a set of comparators for monitoring output of the filters and comparing output to a predetermine threshold and a counter. Haun et al. is silent about the design of the filter and a method of synchronizing an output of the comparators with the counter. Lee at al. teach a switch capacitor bandpass filter. An output of a switched capacitor band-pass-filter (Fig. 5, Pos 334), after comparison on a level comparator 330 is incremented a counter (332) by ANDing with clock (CK). It would have been obvious to

one of ordinary skill in the art at the time the invention to use Lee at al. teachings because use of separately manufactured external filters is much more expensive. Furthermore the filter designed by Lee et al. allow easily synchronize the output with other digital components of the arc fault circuit interrupter.

4. Claims 9, 24,36 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view of Horie et al. (6,054,887). Haun et al. disclose a circuitry (Fig. 1) including a current fault detector circuit 26 and ground fault sensor 20, which comprises operational amplifiers, but silent about a method of correcting an output with offset values. Haun et al. teach an offset voltage correction circuit for an operational amplifier, including steps for comparing an output voltage from the operational amplifier with a prescribed reference voltage, for storing an offset value and for correcting the offset voltage in the operational amplifier in response to the stored digital signal. It would have been obvious to one of ordinary skill in the art at the time the invention to use Horie et al. teachings, because it enable the device to correct the output signals.

Referring to Claim 40, it is inherent that above steps are periodically repeated and therefore offset voltage values are periodically updated.

5. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view of Inoue (5,784,020). Haun et al. disclose a protection system, which analyzes separately several parameters and produces several analog input channels into a microcontroller for further analyzes. Haun et al. did not disclose a way for converting analog signals into digital form. Inoue teaches an analog-to-digital converting device for increasing the number of analog input channels. This device includes a number of the input channels, a multiplexer and A/D converter, which convert an analog signal selected by multiplexer from analog to digital form. It would have been obvious to one of ordinary skill in the art at the time the invention to use teaching of Inoue into design of Haun et al. system, because it allow use of the same A/D converter for converting values of different channels.

6. Claims 14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view of MacKenzie et al. (5,224,006). Haun et al. disclose an ARC Fault Detection System, which produce a trip signal for circuit breaker or other interrupting device, detecting arcing faults and ground faults in an electrical circuit as it was discussed in reference to Claims 1,16 and 28. Haun et al.doesn't disclose a circuit for forming a dormant oscillator neutral detection

system for detecting a grounded neutral. MacKenzie et al. teach an electronic circuit breaker with protection against sputtering ARC faults and ground faults, wherein said ground fault detector means is a dormant oscillator (Claim2). The circuitry of the breaker include two sensors (Fig.3 Pos. 17 and 19) and a group of operational amplifiers/comparators (65,73,73) for comparing to the reference voltage (Col.4, Lines 8-14), where "neutral-to-ground faults couple the current sensing coils 17 and 19 to form a feedback loop around the op amp 65 which causes the op amp 65 to oscillate"(Col.4, Lines 25-32). It would have been obvious to one of ordinary skill in the art at the time the invention to incorporate MacKenzie et al. teachings to an application specific integrated circuit, because it enables the ASIC provide full range of circuit protection.

7. Claims 42-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Haun et al. (6,259,996) in view of Mann et al. (6,185,732). Haun et al. disclose an ARC Fault Detection System, which comprise an application specific integrated circuit, including a micro-controller. Haun et al. doesn't describe a way of testing, monitoring, communicating or debugging internal microprocessor. Mann et al. teach a port installed on a processor-based device with very few pines allowing the processor to communicate through standard JTAG protocol with

external processor or PC. It would have been obvious to one of ordinary skill in the art at the time the invention to include Mann et al. teachings, because it will allow easy control, maintenance and troubleshooting of the ASIC and enable to connect all similar devices to a network for remote testing, monitoring and upgrading software in the microprocessor.

Information Disclosure Statement

8. The information disclosure statement filed 1/17/02 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. It should be mention that foreign patent (B10) 0158365 JP doesn't have the date.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (703) 305-6917. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be

reached on (703) 308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Boris Benenson
Examiner
Art Unit 2836

B.B
December 9, 2002

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800